

electrode constructing the first MOS transistor in the depressed region is set to be larger than that of a margin part of a second gate electrode constructing the second MOS transistor in the ordinary region. A length of the margin part of the second gate electrode is X . The length of the margin part of the first gate electrode is $X + \alpha$ where $0 < \alpha \leq X$.

Through the structure of the claimed invention a) having first and second MOS transistors, each having a margin part and b) the length of the margin part of the first gate electrode is larger by α than that of the margin part of the second gate electrode and where $0 < \alpha \leq X$, as claimed in claim 1, the claimed invention provides a semiconductor device in which an end portion of the first gate electrode completely reaches an upper portion of the insulating film so that the first gate electrode is prevented from partial reduction of the gate length and therefore prevents occurrence of current leakage between source/drain regions which are formed on the exterior of both side surfaces of the first gate electrode. The prior art does not show, teach or suggest first and second MOS transistors each having a margin part where the length of the margin part of the first gate electrode of the first transistor is larger by α than the margin part of the second gate electrode of the second transistor and where $0 < \alpha \leq X$ as claimed in claim 1.

Claim 12 claims a method of fabricating a semiconductor device on the basis of a layout design, the layout design is achieved by a process comprising the steps of; first, designing a layout of an active area on a plane. The active area is defined from an insulating film by a boundary including a first edge extending along a first direction and a second edge extending along the first direction and a third edge connected between one ends of the first and second edges extending along a second direction different from the

first direction. The first to third edges form a step shape so that the second edge is depressed toward an inside of said active area beyond the first edge. Next, a layout of a first gate electrode of a first MOS transistor on the active area is designed. One end of the first gate electrode extends to an outside of the active area across the first edge in a vertical direction to the first direction. Finally, a layout of a second gate electrode of a second MOS transistor on the active area is designed. One end of the second gate electrode extends to an outside of the active area across the second edge in a vertical direction to the first direction. A length y from the second edge to the one end of the second gate electrode is longer than a length x from the first edge to the one end of the first gate electrode where $y = x + \alpha$ where $0 < \alpha \leq x$.

Through the method of the claimed invention having a length y from the second edge to the one end of the second gate electrode being longer than a length x from the first edge to the one end of the first gate electrode, where $y = x + \alpha$ and where $0 < \alpha \leq x$, as claimed in claim 12, the claimed invention provides a method of forming a semiconductor device in which an end portion of the first gate electrode completely reaches an upper portion of the insulating film so that the first gate electrode is prevented from partial reduction of the gate length. The prior art does not show, teach or suggest the method as claimed in claim 12.

Claims 1 and 12 were rejected under 35 U.S.C. § 103 as being unpatentable over *Jassowski et al.* (U.S. Patent No. 5,668,389).

Applicants respectfully traverse the Examiner's rejection of the claims under 35 U.S.C. §103. The claims have been reviewed in light of the Office Action, and for

reasons which will be set forth below, it is respectfully requested that the Examiner withdraws the rejection of the claims and allows the claims to issue.

Jassowski et al. appears to disclose providing more available space by which individual cells may be connected to conductors leading to circuitry outside the cell. (col. 5, lines 7-9) In Fig. 2 a portion of an exemplary cell 9 is shown. The cell 9 is a typical cell of semiconductor devices which may be positioned on a semiconductor substrate as a portion of a group of cells which provide some larger circuit function. The individual cells 9 in each row are each aligned to utilize these power buses so that the power buses 12 and 14 lie within but near to the boundaries of all of the typical cells 9. Once the cells 9 and all other portions of the larger circuit have been laid out, connections are provided between the individual cells 9 and other circuit elements which are carried on the particular substrate. As may be seen in FIG. 2, a single cell 9 includes a number of individual transistor devices created by diffusion of N and P impurities into the substrate, the power conductors 12 and 14, and a series of metallic and polysilicon conductive paths 15 for applying power to the various devices. A great deal of the surface of the cell is covered with these conductive paths 15. In fact, so much of the internal portion of the cell surface is covered by conductive paths that there is very little space for connections to be made to nodes of the cell which must be connected to external circuitry in order for the cell 9 and the circuitry of the group of which it is a part to function correctly. (col. 3, lines 39-61, emphasis added)

Thus, *Jassowski et al.* merely discloses how to provide more space to connect individual cells to conductors and discloses a series of conductive paths 15 for applying

power to the various devices. Nothing in *Jassowski et al.* shows, teaches or suggests a margin part of the gate electrode in a depressed region having a larger length than a gate electrode formed in an ordinary region such that the length of the margin part of the gate electrode in the depressed region is $x + \alpha$ and where $0 < \alpha \leq x$ as claimed in claims 1 and 12.

Applicants respectfully traverse the Examiner's statement that the Applicant has not set forth any explanation for limiting the relationship or set forth any unexpected results. In particular, Applicants obtained the relationship based upon their determination to prevent the occurrence of current leakage between the source/drain regions. In other words, after experimentation, the inventors determined that a relationship as claimed will achieve the goal of preventing shorting between the source/drain regions. Applicants furthermore traverse the Examiner's statement that the relationship is a mere design choice. In particular, page 19, line 23 through page 18, line 9 of the specification discloses one embodiment. The use of the term "for example" discloses the first embodiment. This is not a design choice. Furthermore, Applicants respectfully point out to the Examiner that the claims clearly claim that the length of the margin part in the depressed region becomes $2x$ at the maximum due to the limitation of $x + \alpha$ ($0 < \alpha \leq x$) in the claims. This feature is not shown, taught or suggested by *Jassowski et al.*

Applicants respectfully traverse the Examiner's statement that other portions of the specification support the Examiner's position that the relationship of x and α is merely a design choice by pointing to Figures 3, 6 and 15. Applicants respectfully point out that Figures 3, 6 and 15 represent other embodiments of the present invention and are not design choices.

Applicants respectfully traverse the Examiner's statement that it is immaterial that *Jassowski et al.* does not discuss the prevention of current leakage or adjusting the relational lengths to prevent current leakage. It is respectfully submitted that without knowing how to prevent current leakage or adjust the relational lengths, *Jassowski et al.* would provide any particular lengths to the marginal parts and would not limit the lengths as claimed.

Applicants respectfully submit that the Examiner's position that $x + \alpha$ ($0 < \alpha \leq x$) is just a design choice is only based on a personal point of view and is not supported by the art. The technical principle that the length of the margin part in depressed regions is set to be $2x$ at the maximum as claimed in claims 1 and 12 can not be reached without understanding current defects between source/drain regions. *Jassowski et al.* does not understand these problems, and further, does not disclose or suggest that the length of the margin part should be $2x$ at the maximum.

Applicants respectfully submit that in order to reject the claimed invention the Examiner should present references which clearly point out the problem of current defects between source/drain regions and disclose the structure that the length of the margin part in depressed regions is $2x$.

Since nothing in *Jassowski et al.* shows, teaches or suggests the lengths of the margin parts of the gate electrodes in the depressed or ordinary regions as claimed in claims 1 and 12, it is respectfully requested that the Examiner withdraws the rejection to claims 1 and 12 under 35 U.S.C. § 103.

Since claim 2 depends from a generic claim it is respectfully requested that the Examiner allow claim 2.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested. Should the Examiner find that the application is not now in condition for allowance, it is respectfully requested that the Examiner enters this response for purposes of appeal.

If for any reason the Examiner feels that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, Applicants respectfully petition for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our
Deposit Account No. 02-4800.

Respectfully submitted,

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